A TIME-MULTIPLEX SWITCHING SYSTEM FOR VISUAL DISPLAY OF THE OUTPUTS OF AN ULTRA-SONIC TRANSDUCER ARRAY

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A TIME-MULTIPLEX SWITCHING SYSTEM FOR VISUAL DISPLAY OF THE OUTPUTS OF AN ULTRASONIC TRANSDUCER ARRAY

by

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ABSTRACT

A method of time-multiplexing the output signals from an ultrasonic transducer array for the visual display of an acoustic image by intensity modulation of a cathode ray tube is presented. Considerations pertinent to the design of an all solid-state analog switching system are discussed and the design of a particular system described. Results of tests using simulated signals are presented.

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ACKNOWLEDGEMENTS

The author wishes to express his appreciation to the advisor for this project, Professor G. L. Sackman, for his suggestion of the project and his patience and counsel during the course of work on the project. Additionally, appreciation is extended to Mr. Holly Oren and Mr. Walt Landaker for their assistance in the form of suggestions in the area of hardware assembly for construction of the system.

1. Introduction.

This report presents a method of time-multiplexing the analog output signals of an underwater ultrasonic transducer array onto a common load line for intensity modulation of a cathode-ray tube. This system would be utilized as a subsystem component in an underwater ultrasonic image system under investigation at the Naval Postgraduate School. Results of an experimental investigation of the underwater acoustics portion of the overall system are reported in a thesis by LT K.G. Robinson [1].

The portion of the image system which accomplishes the conversion from acoustical energy to electrical analog signals is comprised of a 9 by 9 square mosaic of piezoelectric transducer elements. Electrical outputs from each of the elements are connected through individual amplifiers which are tuned to the frequency of the transducer. A detector consisting of a diode in series with a capacitor is transformer-coupled to the output stage of each amplifier. Voltage levels in the range from 20 millivolts to 1 volt across the detector capacitor are predicted for the system under investigation. Resultant charge storage permits pulsed operation of the insonifying transducer with the image retained for purposes of readout during the period between transmitted pulses.

Since charge storage by the capacitor is limited only by the inherent reverse leakage current through the diode in the absence of any electrical connection to the detector, it is highly desirable that a readout switch connected to the capacitor have a resistance in the "off" condition which is comparable to the back resistance of the detector diode, to prevent introduction of an additional cause of decay

with time of the detected signal. An additional benefit to be derived from a switch which has this characteristic is the minimization of the error voltage that is generated across a video load by the sum of the leakage currents from the many parallel channels which are in the "off" condition. A further requirement of the switch is that the resistance in the "on" condition should be of a magnitude low enough with respect to the video load impedance that appreciable attenuation of the analog signal does not occur across the switch. Both of these requirements can be met through the use of field-effect transistors operated as solid-state analog switches.

A timing system must provide proper synchronization of the readout of individual elements with electron beam deflection in the display tube. Timing and synchronization of the switches can be provided in a compact form through the use of integrated circuit logic modules. A block diagram of the overall readout and display system is shown in Figure 1.

Selection of the clock frequency at which the individual channels were to be commutated was based on the display of one image frame in the period between transmitted pulses. The maximum range at which the system would be operated in tests in the anechoic pool available at the Naval Postgraduate School dictated a display frame rate of 100 Hz. Original consideration of a 100 element mosaic resulted in a clock frequency of 10 KHz.

More detailed descriptions of design considerations are presented in the subsequent sections of this report.

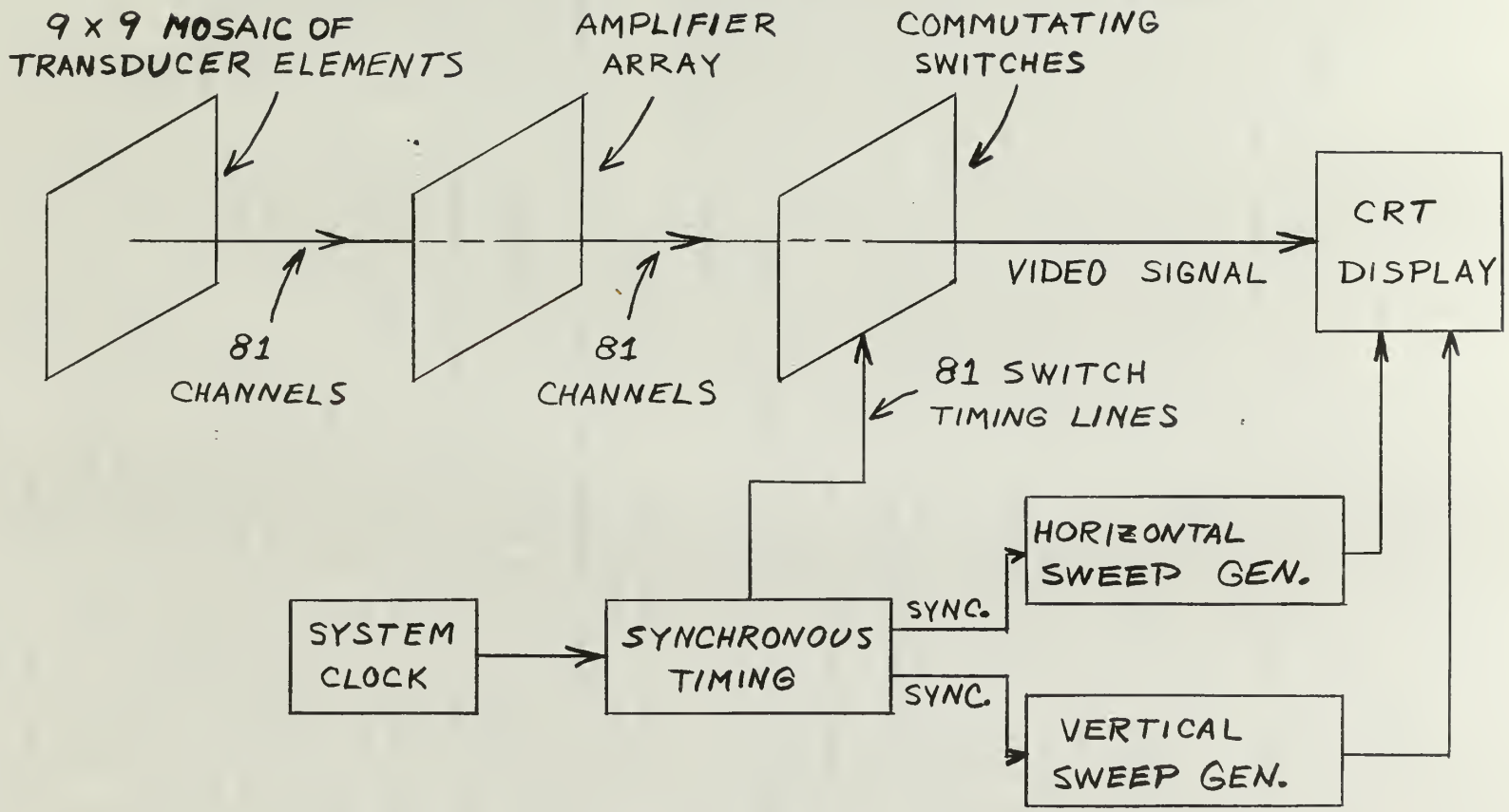


FIGURE 1. BLOCK DIAGRAM OF OVERALL SYSTEM FOR THE DISPLAY OF AN ACOUSTIC IMAGE

2. Logic Circuitry for Timing and Switch Pulse Generation.

Synochronous multiplexing of the analog signals from the individual channels requires a timing and switch pulse generating system to select the channel switches to be opened to the video line in the proper time sequence with the electron beam deflection in the display tube. A number of possible configurations exist for the basic counter in the timing system. Use of a 100 stage ring counter was rejected on the basis of the possibility of cumulative timing errors resulting from propagation delay or pulse overlap. Another possibility was the use of a 7-bit binary coded decimal (BCD) shift register with the required reset logic to produce 100 BCD positions which could be decoded to provide the switch drive pulses in the proper sequence. Anticipated horrendously tedious wiring interconnections for a seven stage shift register and subsequent decoding logic circuits, if this latter configuration were used, prompted the search for a simpler system by which the necessary timing could be provided for the image system under investigation.

Since the receiving transducer-amplifier array could be viewed as a 10 by 10 square array of positions to be decoded in the 100 channel system originally under consideration, a seemingly natural approach to the design was the use of 2 decimal counters, one for the column position and one for the row position, with suitable logic circuitry for combination of the output states of the two counters to provide channel position decoding in the proper time sequence. A diode decoding matrix or an array of two-input logical "AND" gates could be used to obtain the necessary decoding functions on the basis of column-row coincidence. The number of diodes required in a diode decoding matrix would be much larger than the number of

integrated circuit logic gates and would also introduce the problem of logic level attenuation due to the voltage drop across the diodes when in the forward biased condition. Accordingly, a decision was made to use logic gates to perform the element position decoding function. A block diagram representation of the relationships between the 2 decimal counters and the array of decoding gates is shown in Figure 2. In the figure $Z_{(X_i,Y_j)}$ refers to the output of the decoding matrix which provides the timed driving pulse to the switch which in turn connects the channel in the (X_i,Y_j) position to the video display line. Since the experimental mosaic was reduced to 9 by 9 elements as a result of certain practical limitations, the number of channels to be commutated was reduced to 81, thus requiring only 81 switch timing signals. The tenth column and row positions for the 100 channel system, $Z_{(X_9,Y_j)}$ and $Z_{(X_i,Y_9)}$ respectively, were therefore available to synchronize the display tube deflection circuit retrace periods with the readout timing.

An objective in the design and construction of the timing system was to make use of available integrated circuits to reduce the size of the system required. Many different types of integrated circuit logic modules were commercially advertised at the time that the project was begun. Selection of which type would be used was made on the basis of the availability of certain modules at the Naval Postgraduate School. This allowed assembly of designed circuitry for the purpose of checkout of logic design validity and of the switch drive capability of the logic gates. Logic modules available were elements from the Fairchild Semiconductor Industrial Micrologic Integrated Circuit line. Additional considerations were the low cost of these units in the epoxy encapsulated

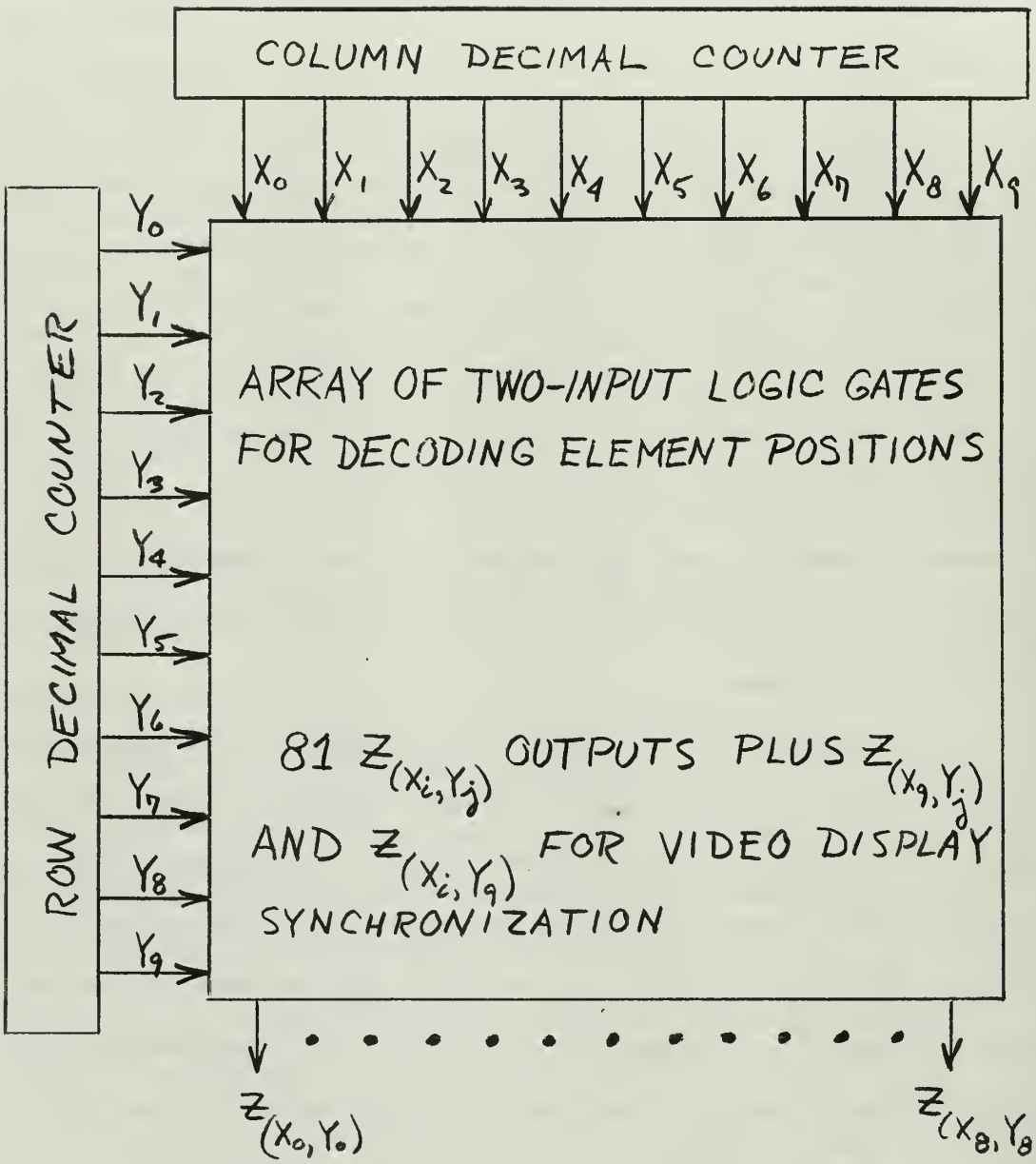


FIGURE 2. BLOCK DIAGRAM REPRESENTATION OF SYSTEM USED TO GENERATE CHANNEL SWITCH TIMING PULSES.

form and the availability of elements in sufficient quantities to complete construction of the system. The elements in this line of logic modules form a compatible family of resistor-transistor logic (RTL) components with a high noise immunity and a high drive or "fan-out" capability. Positive logic was assumed throughout the timing and switch pulse generating circuitry. In this logic system, a high output level from a logic element corresponds to a logical "1" or true condition and a low output level to a logical "0" or false condition. Information relating to the logic modules used in the design and construction of the timing system is contained in Appendix I.

Block diagrams of the logic circuitry for the binary coded decimal shift registers and the binary-to-decimal decoders which make up each of the 2 decimal counters are shown in Figures 3 and 4 respectively. Outputs and complements from the 4 flip-flops in each of the registers are connected through buffer-inverter amplifiers to remain within the "fan-out" limitations specified for the 923 JK flip-flops by the manufacturer. The shift register reset logic shown in Figure 3 serves to cause the JK flip-flops to function as trigger flip-flops by controlling the times at which the outputs undergo a change of state as a function of the occurrence of the clock pulses for either of the shift registers. Dashed blocks indicate the use of a single 914 dual two-input gate to perform the function indicated within the block. Outputs of the binary-to-decimal decoding gates are also connected through buffer-inverter amplifiers to remain within specified "fan-out" limits set for the 914 gate. This feature also performed the function of logic level inversion required to obtain a positive logic level at the outputs of the individual element position decoding gates for a given

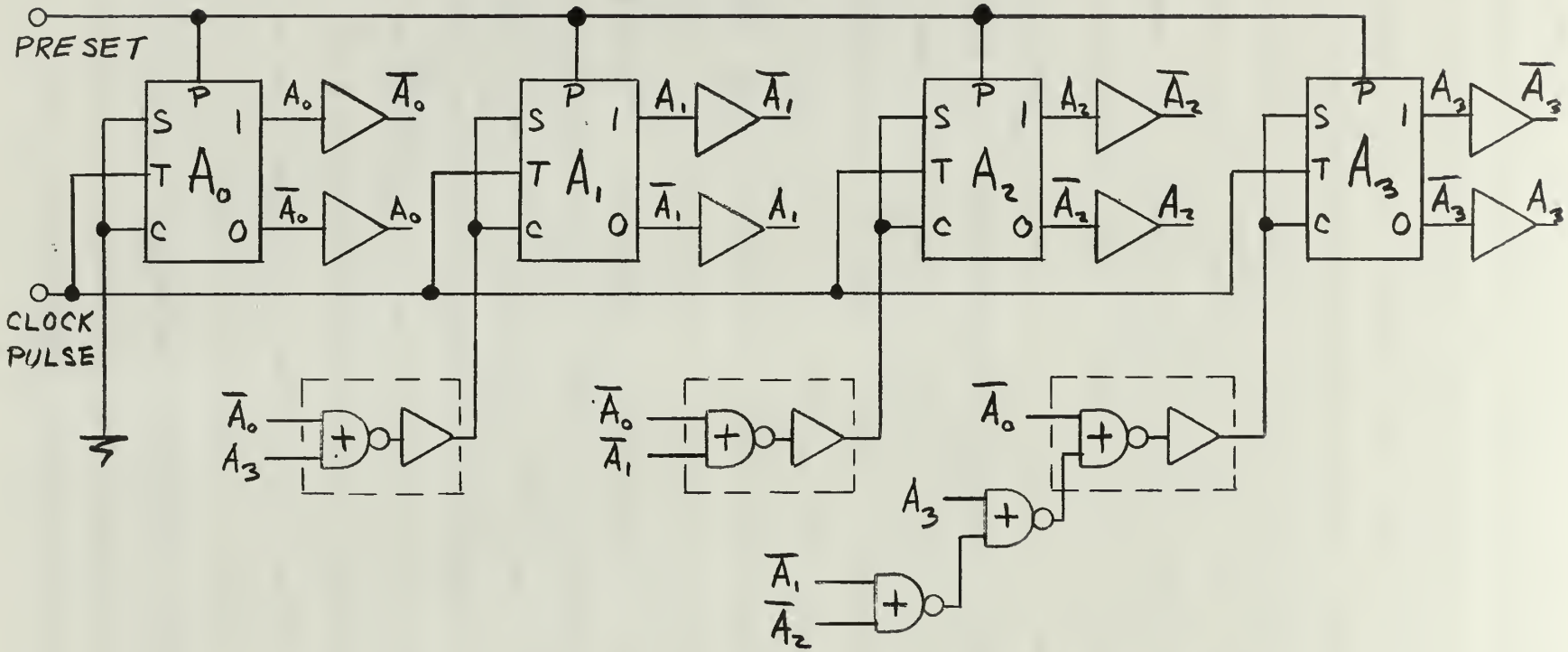


FIGURE 3. BLOCK DIAGRAM OF BINARY CODED DECIMAL DECADE COUNTER SHIFT REGISTER

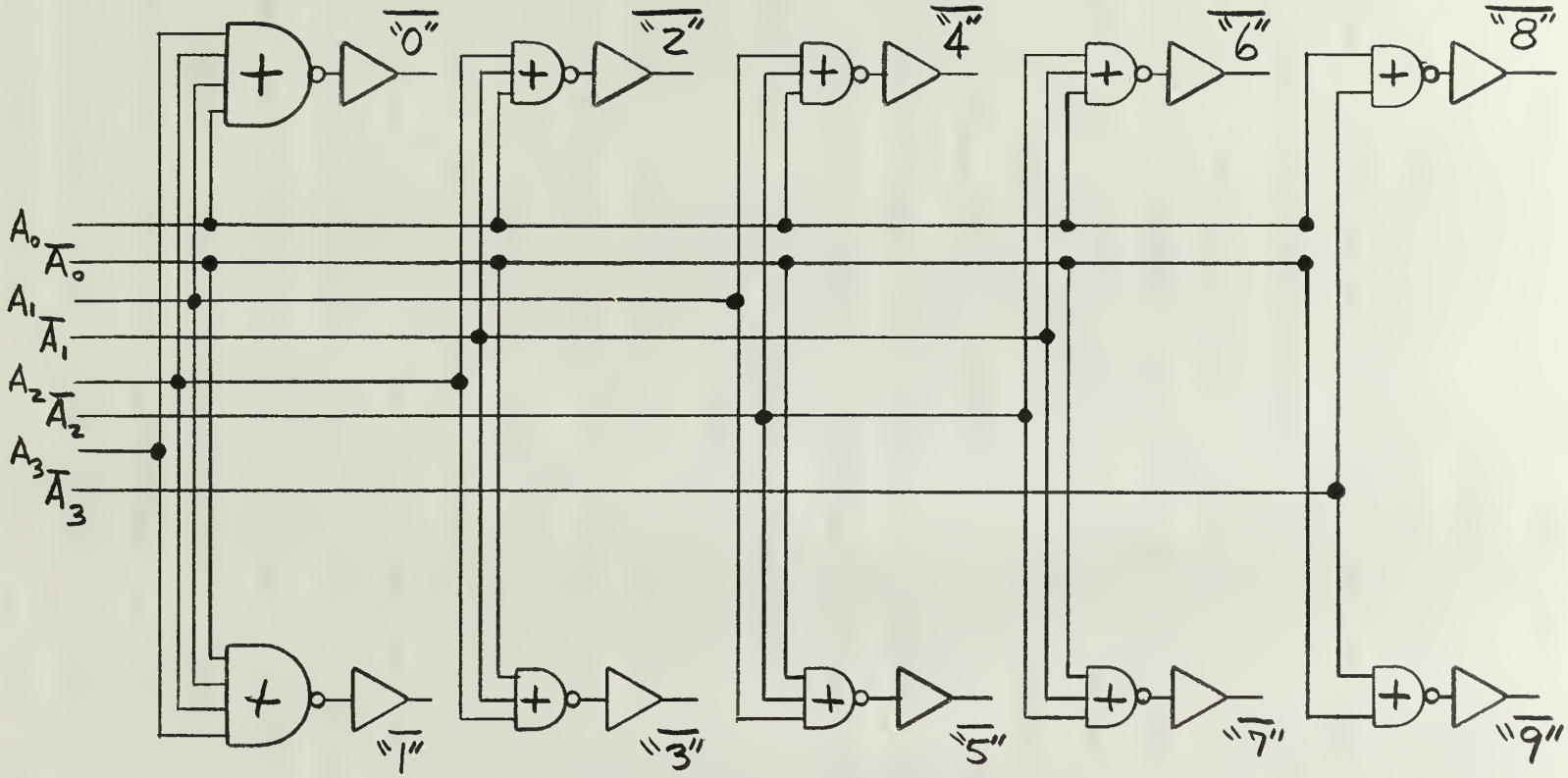


FIGURE 4. BLOCK DIAGRAM OF BCD TO DECIMAL DECODER FOR DECADE COUNTER BCD SHIFT REGISTER

column-row coincidence (the 914 gate operates as a "NOR" gate for positive logic). Liberal application of DeMorgan's Laws of Boolean Algebra at this stage in the design was the only recourse by which the author was able to retain even slight presence of mind in the course of determining the proper element interconnections to obtain the desired functioning. The clock pulse for the column counter is furnished by an external pulse generator operating at the clock frequnecy chosen for commutating the individual channels and the clock pulse for the row counter is derived from the buffered output of the A_3 flip-flop in the column counter. This latter arrangement is necessitated by the fact that the 923 JK flip-flop is responsive only to a negative going transient on the clock pulse terminal subject to the levels at the set and clear terminals as stated in Appendix I.

Outputs from the 2 decimal counters described above are connected to a matrix of decoding gates, the outputs of which are in turn connected directly to the individual channel switch modules. A block diagram which depicts the interconnections between the decoding gates and the switch modules and the individual channel signal input lines for the first row of the array is shown in Figure 5. The outputs of the decoding gates provide the synchronized switch driving pulses for the switch modules directly as a result of the inherent ability of the logic gates to supply the necessary base drive current for the junction transistors used to control the field-effect transistor switches.

A disadvantage resulting from the use of NOR gates as the channel decoding gates in a system for which positive logic is used is that, at any particular time, only one of the gates is operated in the unsaturated state. This condition imposes a heavy current drain on the low voltage

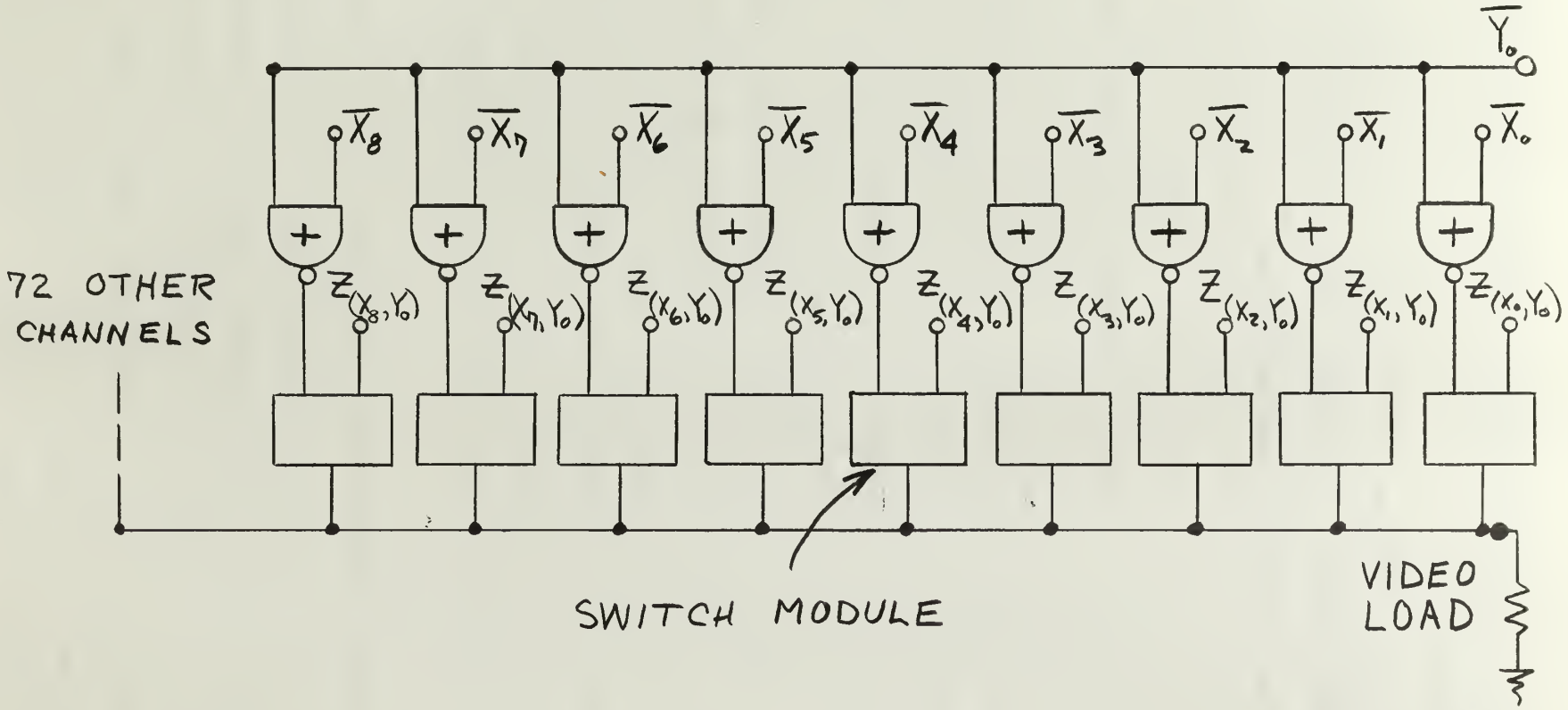


FIGURE 5. BLOCK DIAGRAM OF INTERCONNECTION OF LOGIC DECODING GATES AND CHANNEL SWITCH MODULES FOR FIRST ROW OF ARRAY.

power supply for the timing system (1.6 amperes at 3.6 volts for the system constructed).

The timing subsystem in its completed form is composed of 114 logic modules mounted on 19 printed circuit cards which are enclosed in a single 19 inch relay rack card holder.

3. Description of Analog Signal Switching Circuitry

The type of switch to be used in any contemplated analog signal switching system for multiplexing the output signals from the transducer-amplifier array has imposed upon it three requirements. First of all, the switch must have a high impedance in the "off" condition to minimize decay of the detector output level due to leakage current through the switch during the periods between target returns. Secondly, minimal attenuation of the signals to be passed by the switch when in the "on" condition is necessary in view of the relatively low output levels predicted for the system. Stated in another way, the "on" resistance of the switch must be lower than the input impedance of the video load line by at least an order of magnitude. The third requirement which is in actuality a desireability to reduce the complexity of the switching circuitry, is that there should be no "offset" voltage betwen the input and output terminals of the switch when in the "on" condition as a result of a bias voltage required to operate the switch in this condition. In addition, it is apparent from the large number of switches required that the circuit complexity and cost of the individual switches should be held to the minimum required to perform the desired functions.

Availability of relatively inexpensive 2N 4360 "p-channel" junction field-effect transistors (JFET'S) provided a means of meeting the requirements and desirable characteristics outlined above. The very low (typically .15 nanoamperes) gate-to-drain reverse leakage current of this particular silicon device, with the gate-to-drain and gate-to-source junctions biased at a voltage greater than the "pinch-off" voltage (V_P) which is required to effectively cut off conduction

from drain to source, minimizes a source of error voltage in the common video load due to the sum of the reverse leakage currents from the 80 channel switches in the "off" condition at any one time. A drain-to-source resistance (which is variable among different transistors and with gate-to-source bias) in the range of 350 to 700 ohms with the switch in the "on" condition meets the requirement of minimal attenuation of the analog signals, since the input impedance of the emitter-follower stage normally used prior to the video driver stage would be of the order of 10K ohms. Characteristics of the 2N 4360 relevant to analog switching applications are described in Appendix II.

The circuit configuration used for the individual switch modules shown in relation to the decoding gates in Figure 5 is shown in Figure 6. In the absence of a switch driving signal from the decoding gate, the switch drive transistor is maintained in the "cutoff" condition which causes the FET switch to be maintained in the "off" condition as a result of the gate bias voltage provided by the collector supply voltage of the driver transistor. An emitter circuit resistor is included to maintain the gate-to-source junction voltage at a sufficient level to prevent this junction from becoming forward biased in the "on" condition to the point at which gate current would be drawn from the detector capacitor. If this condition were to occur, excessive discharge of the detector capacitor during the period of channel signal readout would result at the higher anticipated analog signal levels. Another means of accomplishing this same end result would be to include a parrallel combination of a diode and a capacitor in the circuit from the collector of the drive transistor to the gate terminal of the switch transistor with the diode positioned such

that its forward bias direction is toward the gate terminal. In this case the emitter circuit resistor can be eliminated. This modification maintains the gate at approximately the same voltage as the source whenever the source voltage exceeds the collector-emitter saturation voltage of the drive transistor, thereby effectively isolating the gate terminal for the conditions described. A base input resistor was not used in the base circuit of the drive transistor in order to maintain simplicity of switch module circuitry and to achieve better transient response of the drive transistor during turn-on and turn-off without the use of resistor-capacitor rise-time compensation in the base circuit. This was possible on the basis of the logic circuitry operating voltage and the circuitry of the decoding gates. As a result, base current in excess of that required to drive the switch transistor into saturation is supplied by the logic gates, but is not of a magnitude which would result in damage to the transistor.

An inherent problem in the use of field-effect transistors as analog switches in a multi-channel system is the coupling of gate drive signals to the common load by the gate-to-drain capacitance. The problem arises primarily when the gate drive signal acts to turn off the FET switch and this capacitance charges toward the value of the off condition bias voltage. Voltage "spikes" occur across the load as a result. These transients decay with a time constant determined primarily by the series combination of the drive transistor collector circuit resistor plus the load impedance and the value of the gate-to-drain capacitance. For the component values in the switch module configuration shown in Figure 6 these voltage "spikes" did not present a problem except at the lower input signal levels and even then decayed

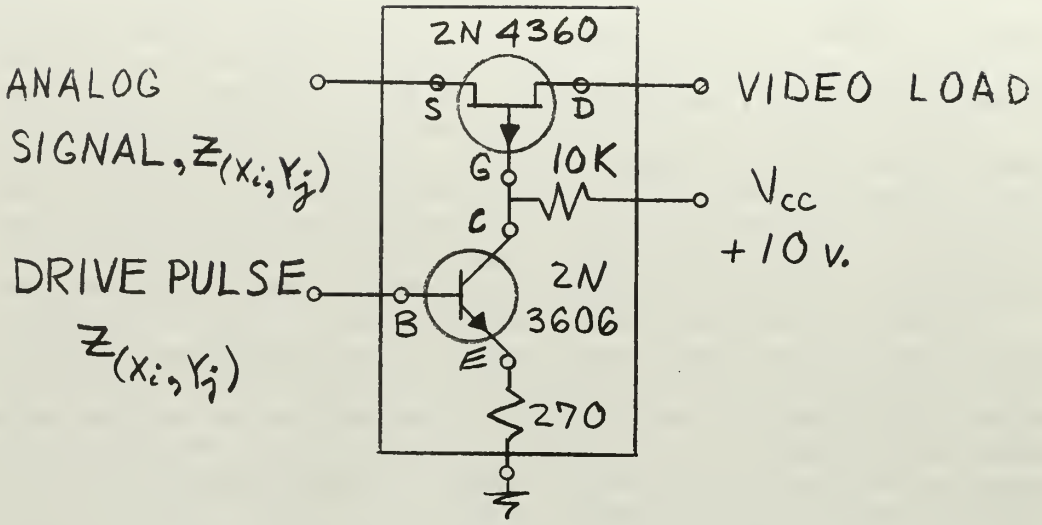


FIGURE 6. ANALOG SWITCH MODULES FOR INDIVIDUAL CHANNELS

rapidly enough to be considered insignificant. The switch modules are mounted in groups of nine on printed circuit cards requiring a total of nine cards for the analog switching circuitry.

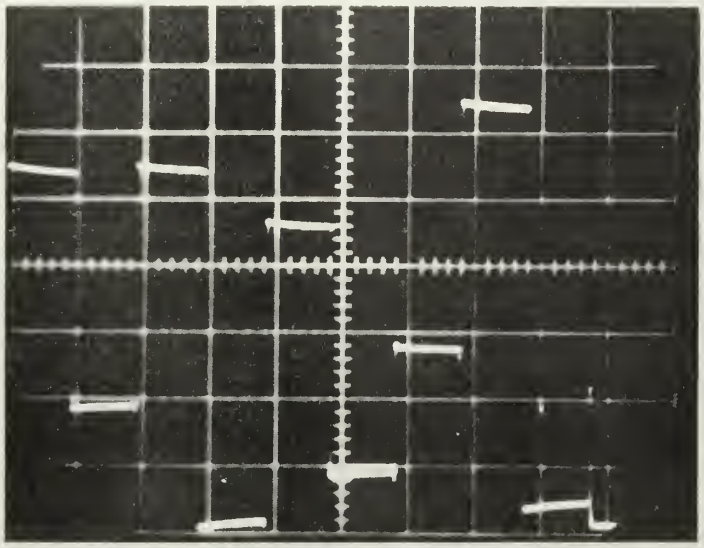
4. Experimental Results.

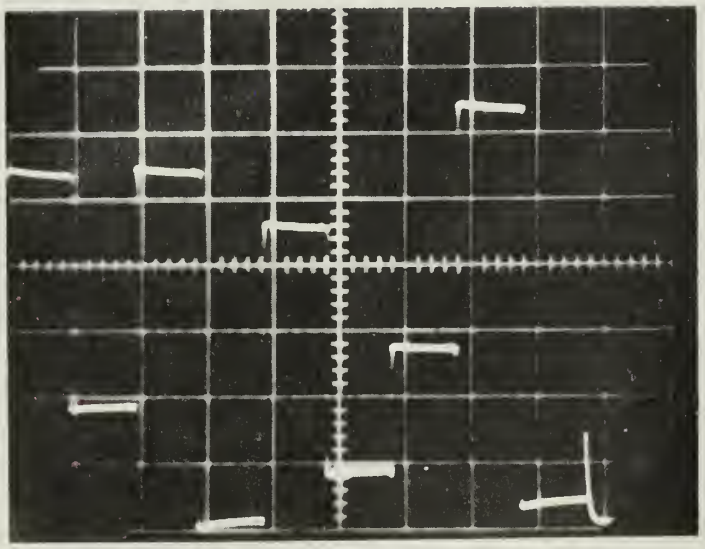
Since construction of all of the subcomponents of the image system under investigation was not completed in sufficient time to permit assembly for checkout of system functioning, performance of the analog switching circuitry was tested by simulation of a range of anticipated signal levels. These levels were generated by the use of a group of 9 potentiometers paralleled across a voltage supply. The potentiometers were adjusted to produce a pattern of levels which were in turn connected to the switch input terminals of the switch modules for the element positions corresponding to the first row of the transducer array. Resulting time-multiplexed waveforms observed on the common video line are shown in Figures 7 (a) and 7 (b). The zero voltage reference corresponds to the lower reticle line in the figures. The sequence of channel outputs shown is in the order $Z_{(X_0,Y_0)}$ through $Z_{(X_8,Y_0)}$. Input signal levels were nominally .6, .2, .6, .02, .5, .1, .3, .7 and .05 volts in the same sequence. No particular significance should be attached to this pattern since it was selected merely to observe the switching characteristics. In Figure 7 (b) a 500 picofarad (pf.) capacitor was connected in parallel with the simulated video load to approximate the total capacitance in shunt with the load which would result if all of the switches were connected and operated. This value of capacitance was selected on the basis of the nominal value of 5 pf. for the output capacitance of each of the FET switches in the other 72 channels which were not in operation, with the additional amount added to account for the stray capacitance inevitably present. The magnitudes of the simulated signals indicated above were values measured prior to connection to the input terminals

of the switches. Hence, the observed values are less than the simulated levels both due to the effect of the load resistance paralleled with the wiper-arm to ground resistance of the potentiometers and attenuation due to the drain-to-source resistance of the FET switches. The former effect is predominant as a result of the total resistance value of the potentiometers used. However, the effect of capacitive shunting of the load is clearly evident. The turn-off "spikes" observed are not considered to be a source of serious problems in the visual display of the multiplexed waveforms, since the duration of these "spikes" is short compared to the time per element readout.

In the course of the simulation described above, the frequency capability of the constructed unit was also examined. The unit operated up to 10 MHz, the maximum frequency attainable with the pulse generator used as the clock pulse source in the tests, with moderate deterioration in the rise time response. Some of the noted deterioration in performance could obviously be traced to the performance of the oscilloscope used which had a frequency response rated at 450 KHz.

During early phases of the design of the switch circuit, tests were also made to ascertain the effect of channel readout through the switch on the charge storage of the individual channel detector. Using an amplifier and detector identical to those used in the amplifier array, readout of the detector level resulted in a 10-20% reduction in the detector voltage. This reduction is a direct function of the time per element readout and the value of the video load impedance. Reasons for interest in this property of the switch circuit is that it would be desirable that the readout process be as nearly non-destructive as possible for operation of the system at longer ranges. This results





from a consideration of effects on the displayed image when the array is scanned more than once in the interval between object returns. A design comprimise is necessary in this respect, however, since an increase in the video load impedance results in larger turn-off "spikes" and an increase in the turn-off time of the individual channel switches. The readout time per element is a function of the frame rate chosen. Increase in the frame rate is, therefore, another method of reducing the degree of destructive readout for operation at longer ranges.

5. Conclusions.

It is possible to design a solid-state, multi-channel multiplexing system meeting the requirements for application to visual display of the analog signal outputs of an acoustic image system transducer array. Relatively simple circuitry is possible through the use of integrated circuit logic modules for system timing and synchronization and field-effect transistors operated as analog switches. As larger arrays are considered to obtain a correspondingly larger field of view, integrated circuit techniques should be directly applicable to the fabrication of the entire timing and switching circuitry to reduce overall size.

The use of resistor-transistor logic in the particular system which was designed and constructed provided a means of simplifying the switch drive circuitry, but resulted in a requirement for a power supply for the timing circuitry which was capable of supplying high current at low voltage (1.6 amperes at 3.6 volts). This requirement arose primarily due to the use of NOR gates to provide the individual switch driving pulses in a system based on positive logic. Under this logic system the individual gates are normally maintained in the saturated condition except for the time that the gates provide a timing pulse. A solution to the problem of power supply requirements, particularly in the event that a larger system were to be constructed using the same type of components and logic system, would perhaps be to subdivide the system and use a separate power supply for each subsystem block of components. The use of FET switches operated as analog switches poses an inherent problem of coupling of the switch gate drive pulses to the common load. However, the magnitude and duration of the resulting transients are not considered to pose a serious problem with

respect to the effect on the displayed image as a result of the duration of the transients in respect to the time per element readout. An error voltage across the video load also results from the sum of the leakage currents from the off channels, but the total effect is minimized by the relatively low leakage currents of the FET. Compensation of this error voltage could be made in the video circuits of the display tube. The degree of "destructiveness" of the readout of the channel detector levels is not a problem for the ranges at which the image system will be initially tested. As the range of operation is increased beyond tnat attainable in the available anechoic pool, increase in the display rate is possible to reduce the degree of destructive readout.

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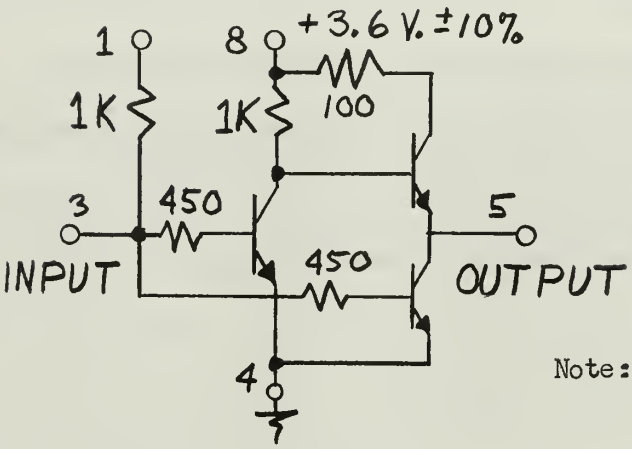
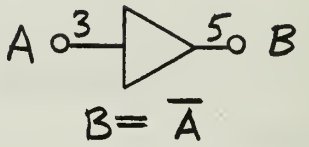
Appendix I

Description of Logic Modules.

a. 900 Buffer-Inverter Amplifier



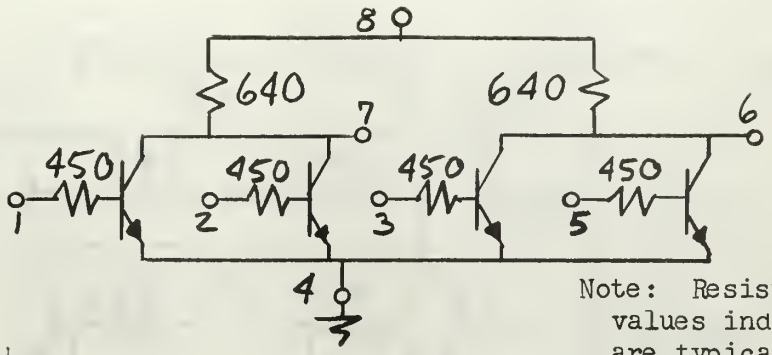
LOGIC SYMBOL



Note: Resistance values indicated are typical values.

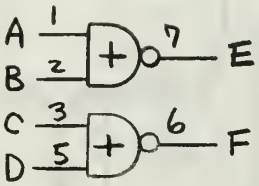
The Fairchild Micrologic 900 medium power buffer-inverter element is a low impedance inverter-driver capable of supplying 16 ma of current at .9 v at its output terminal. Low source impedance permits high fan-out and minimization of risetime deterioration due to capacitive loading in line drive applications. Fan out capability is 80 load units. The input terminals of any of the elements in the Fairchild medium power group are represented by a load factor of three load units.

b. 914 Dual Two-Input Gate

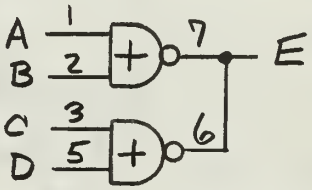


Note: Resistance values indicated are typical values.

LOGIC SYMBOL(S)



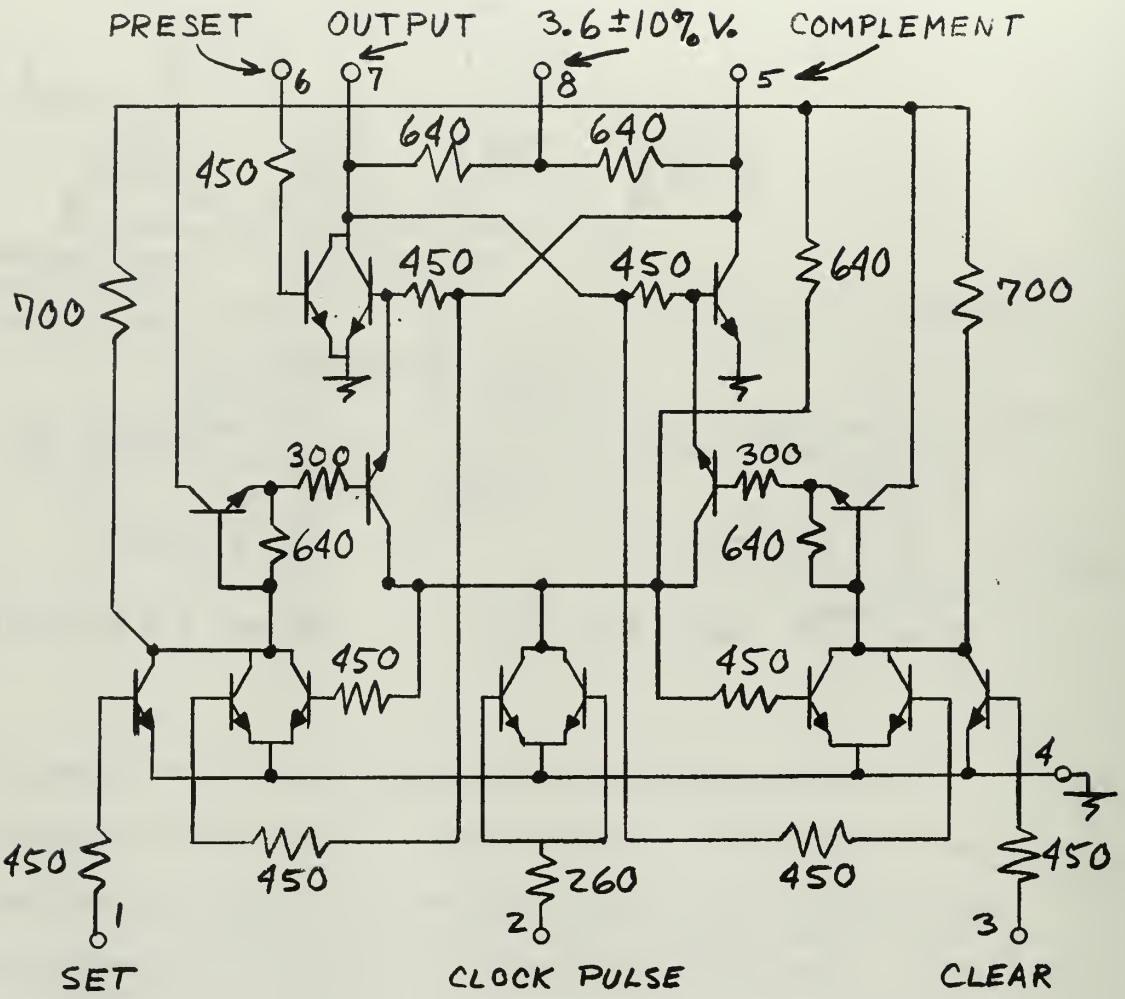
OR



$E = \overline{A+B}$ AND $F = \overline{C+D}$ $\qquad E = \overline{A+B+C+D}$

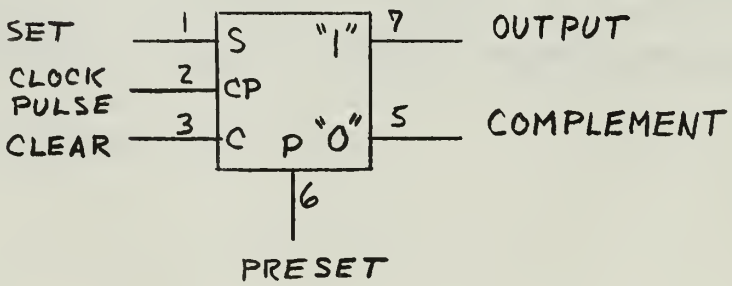
The Fairchild Micrologic 914 dual two-input gate operates as a logical NOR gate for positive logic. It is possible to generate any logic function through the exclusive use of these dual two-input gates. Either gate can be used as an inverter by interconnecting the two inputs or by grounding one input. A fan-out capability of 16 load units for each of the output terminals is specified by the manufacturer when the gates are operated independently or 30 load units when the outputs are interconnected to form a four-input gate. Maximum propagation delay is rated at 32 nanosec.

c. 923 JK Flip-Flop



Note: Resistance values indicated are typical values.

LOGIC SYMBOL

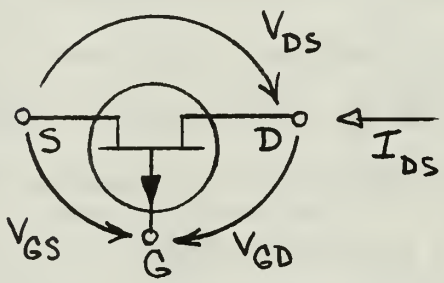


The Fairchild Micrologic 923 JK flip-flop is designed for industrial shift register and binary counting applications at frequencies up to a 2 MHz. Change of the logic level at the output is produced by a falling transient at the clock pulse terminal subject to the levels present at the SET and Clear terminals as enumerated below. If the level at both the S and C terminals is high, the state of the output is not changed by the occurrence of a trigger pulse. On the other extreme, if the level at both the S and C terminals is low, the output state is reversed by the occurrence of a trigger pulse. By connecting the S and C terminals in common to the output of a logic gate it is therefore possible to operate the 923 element as a trigger flip-flop. A low level on the S terminal and a high level on the C terminal causes the output to assume a low level upon occurrence of a trigger pulse. For the condition when the S level is high and the C level low, the output assumes a high level upon occurrence of a trigger pulse. A positive level applied to the PRESET terminal sets the output level to the low level. Fan out on either the output or complement terminals is 10 load units. Maximum propagation delay time for this module is 80 nanosec.

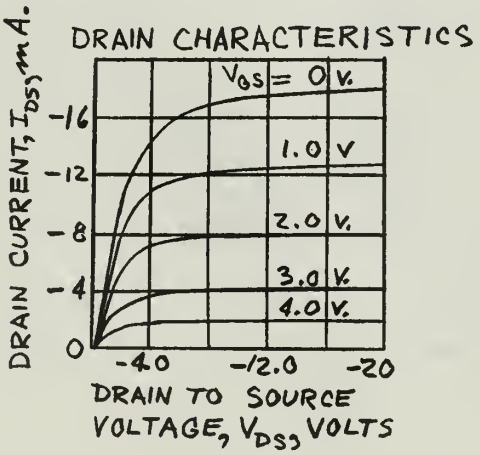
APPENDIX II

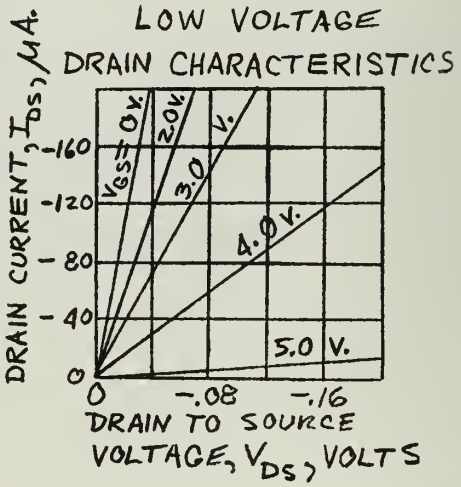
Characteristics of the 2N 4360 p-channel field-effect transistor relevant in application to analog switching operations.

a. The symbolic representation of a p-channel junction field-effect transistor is shown below with the directions of conventional voltage and current indicated:



b. Typical drain electrical characteristics at 25° C. are shown in the figures below. The region of interest for operation of the device as an analog switch is the low level portion of the curves where the drain current and voltage are proportional, i.e., the device is resistive.





c. Typical electrical characteristics at 25°C. as specified by the manufacturer are tabulated below:

Symbol	Characteristic	Min	Typical	Max	Test Conditions
BV_{GSS}	gate-to-source breakdown voltage (volts)	20			I_G = 10 μamp. V_{DS} = 0 v.
I_{DSS}	drain current (milliamps)	3.0	10	30	V_{DS} = -10 v. VGS = 0 v.
$V_{GS(off)}$	gate-to-source cutoff voltage (volts)		5.5	10	V_{DS} = -10 v. I_{DS} = 1.0 μamp.
I_{GSS}	gate reverse current (namp.)		.15	10	V_{GS} = 15 v. V_{DS} = 0 v.
C_{iss}	input capacitance (pf. at f=1.0 MHz)		15	20	V_{DS} = -10 v. V_{GS} = 0 v.
C_{rss}	reverse transfer capacitance (pf. at f=1.0 MHZ)		3	5	same conditions as for C_{iss}
$r_{ds(on)}$	drain on resistance (Ωat f = 1.0 KHz)		350	700	V_{DS} = -10 v. V_{GS} = 0 v.

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13. ABSTRACT

A method of time-multiplexing the output signals from an ultrasonic transducer array for the visual display of an acoustic image by intensity modulation of a cathode ray tube is presented. Considerations pertinent to the design of an all solid-state analog switching system are discussed and the design of a particular system described. Results of tests using simulated signals are presented.

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14. KEY WORDS	LINK A		LINK B		LINK C	
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